

**ANDREWS**  
ATTORNEYS  
**KURTH LLP**



111 Congress Avenue, Suite 1700  
Austin, Texas 78701  
512.320.9200 Phone  
512.320.9292 Fax  
andrewskurth.com

Pamela Menke  
512/320.9228 Direct

April 16, 2004

**VIA US EXPRESS MAIL**

MAIL STOP DD  
Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Re: App No. 10/814,532; "Integrated Circuit Stacking System and Method"  
Docket No. 0254-094-PCT-2-USCIP-1

Dear Commissioner:

Please find enclosed for filing the following:

1. Information Disclosure Statement;
2. Form 1449 (and one duplicate copy);
3. 104 references; and
4. a return postcard for confirmation of receipt.

The Commissioner is hereby authorized to charge any fees which may be required to Deposit Account 50-0897. Please return the postcard confirming your receipt of the enclosed materials.

Yours truly,

ANDREWS & KURTH LLP

  
Pam Menke

Board Certified Legal Assistant in Civil Trial Law  
Texas Board of Legal Specialization

/pm  
enclosures



Attorney Docket No.: 0254-094-PCT-2-USCIP-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: Integrated Circuit Stacking System and Method

Application No.: 10/814,532

Filing Date: 03/31/2004

Inventor: Cady, et al.

Assignee: Staktek Group, L.P.

Examiner: TBA

Group: TBA

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (six sheets) with references listed for consideration by the Office.

In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

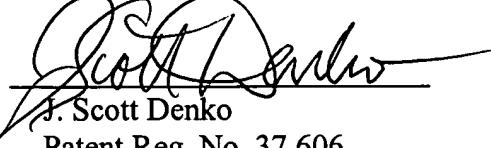
In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. §§ 102 or 103.

This Information Disclosure Statement is being filed before receipt of the first Office action, so no fee is believed to be due. The Commissioner is hereby authorized to charge any fees which may be required in connection with the filing, or to credit any overpayment to Deposit Account No. 50-0897, upon which account the undersigned has the authority to sign. A **duplicate copy of Form 1449 is enclosed.**

Respectfully submitted,

April 16, 2004  
Date

ANDREWS & KURTH LLP

By: 

J. Scott Denko  
Patent Reg. No. 37,606  
111 Congress Ave., Suite 1700  
Austin, Texas 78701  
(512) 320-9200 Telephone  
(512) 320-9292 Facsimile

Form PTO-1449 (Modified) (Rev. 11/92) <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use several sheets if necessary) (37 CFR 1.98(b))				U.S. Dept. of Commerce Patent and Trademark Office		ATTY. DOCKET NO.	SERIAL NO.
						0254-094-PCT-2-USCIP-1	10/814,532
				APPLICANT		Cady, et al	
				FILING DATE		GROUP	
				3/31/04			
				<b>U.S. PATENT DOCUMENTS</b>			
*Examiner Initial	Patent Number		Patentee	Class	Subclass	Filing Date (if appropriate)	
	6,222,737B1	4/24/2001	Ross, Andrew C.	361/767		4/23/1999	
	6,360,433B1	3/26/2002	Ross, Andrew C.	29/840		9/19/2000	
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	6,097,087	8/1/2000	Farnworth, Warren M. et al	257/698		10/31/1997	
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	6,514,793B2	2/4/2003	Isaak	438/109		2/4/2003	
<b>FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION</b>							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	58-96756(A)	06/08/1983	Japan			Partial	
	58-112348(A)	07/04/1983	Japan			Partial	
	60-254762	12/1985	Japan			Partial	
	EP 0 298 211 A#	01/11/1989	European			X	
<b>OTHER DOCUMENTS</b> (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)							
		Dense-Pac Microsystems, Breaking Space Barriers, 3-D Technology 1993					
		Dense-Pac Microsystems, DPSS12X16A3, Ceramic 512K X 16 CMOS SRAM Module					
		“Design Techniques for Ball Grid Arrays,” William R. Newberry, Xynetix Design Systems, Inc.					
EXAMINER				DATE CONSIDERED			
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(37 CFR 1.98(b))				FILING DATE	GROUP
				3/31/04	

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	6,262,895 B1	7/17/2001	Forthum, John A.	361/749		1/13/2000
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	6,300,679B1	10/9/2001	Mukerji et al.	257/738		6/1/1998
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	6,590,282B1	7/8/2003	Wang et al.	257/686		4/12/2002
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	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	62-230027(A)	10/08/1987	Japan			Partial	

**OTHER DOCUMENTS**  
*(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)*

	"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.
	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division
	"High Density Memory Packaging Technology High Speed Imaging Applications," Dean Frew, Texas Instruments Incorporated
	Teresa Technologies, Inc. – Semiconductor Intellectual Property, Chip Scale Packaging – Website pages (3)

EXAMINER

DATE CONSIDERED

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<b>U.S. PATENT DOCUMENTS</b>							
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)	
	6,473,308B2	10/29/2002	Forthun	361/749		04/19/2001	
	US2002/0006032A1	01/17/2002	Karabatsos	361/760		01/11/2001	
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	4,513,368	04/23/1985	Houseman	364/200		05/22/1981	
	4,645,944	02/24/1987	Uya	307/243		09/04/1984	
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<b>FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION</b>							
Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
<b>OTHER DOCUMENTS</b> <i>(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)</i>							
		"Tessera Introduces uZ™ - Ball Stacked Memory Package for Computing and Portable Electronic Products" Joyce Smaragdis, Tessera Public Relations; 2 figures that purport to be directed to the uZ™ - Ball Stacked Memory Package.					
		Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.					
		Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory, 1 Page.					
		"Vertically-Integrated Package." Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University					
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				<b>FILING DATE</b>		<b>GROUP</b>	
3/31/04							
<b>U.S. PATENT DOCUMENTS</b>							
*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)	
	6,620,651B2	9/16/2003	He et al.	438/113		10/23/2001	
	US2002/0139577A1	10/3/2002	Miller, Charles A.	174/261		3/27/2001	
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<b>FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION</b>							
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						Yes	No
<b>OTHER DOCUMENTS</b> (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)							
		Dense-Pac Microsystems, 256 Megabyte CMOS DRAM DP3ED32MS72RW5					
		IBM Preliminary 168 Pin SDRAM Registered DIMM Functional Description & Timing Diagrams					
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<b>U.S. PATENT DOCUMENTS</b>							
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*Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if appropriate)
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